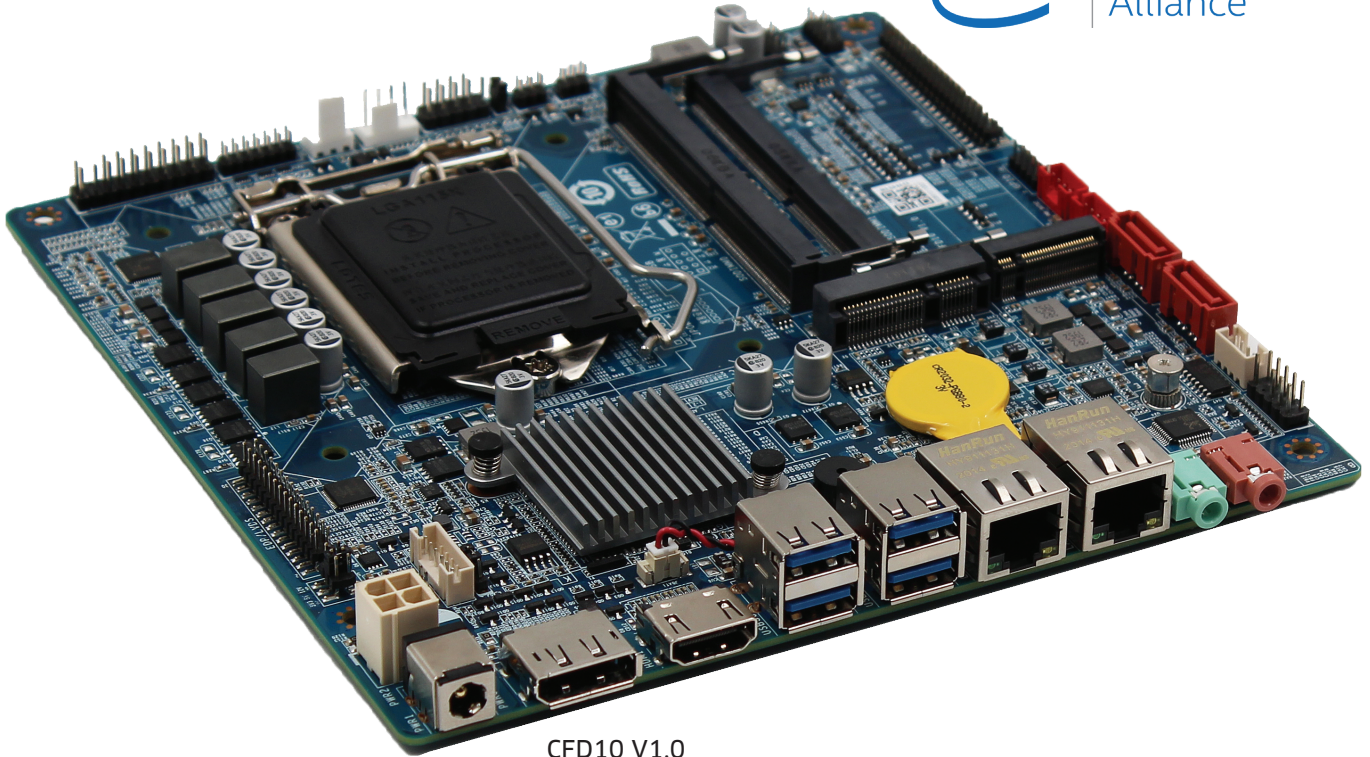


CFD10

Mini ITX based on the H310 chipset and Intel Coffee Lake CPU (FCLGA1151)



IoT Solutions
Alliance



CFD10 V1.0

Features

- CPU: Intel Coffee Lake LGA1151 CPU
- Memory: Dual channel SO-DIMM DDR4 (max 64 GB)
- Display: 2x HDMI, 1x DP, 1x LVDS (eDP optional)
- Ethernet: Support dual 1GbE ethernet cards
- Expansion: M.2, Mini PCIe
- Power: 12V DC input
- Security: TPM 2.0 supported (optional)



H/W Monitor



Watchdog



GPIO



Brightness

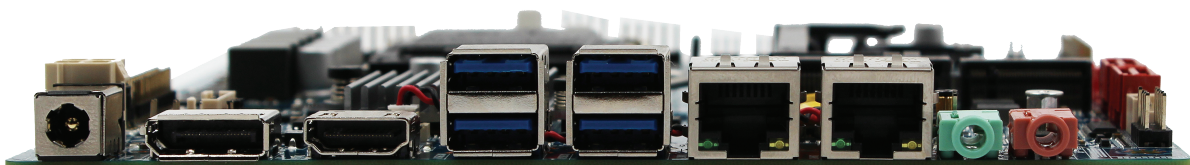
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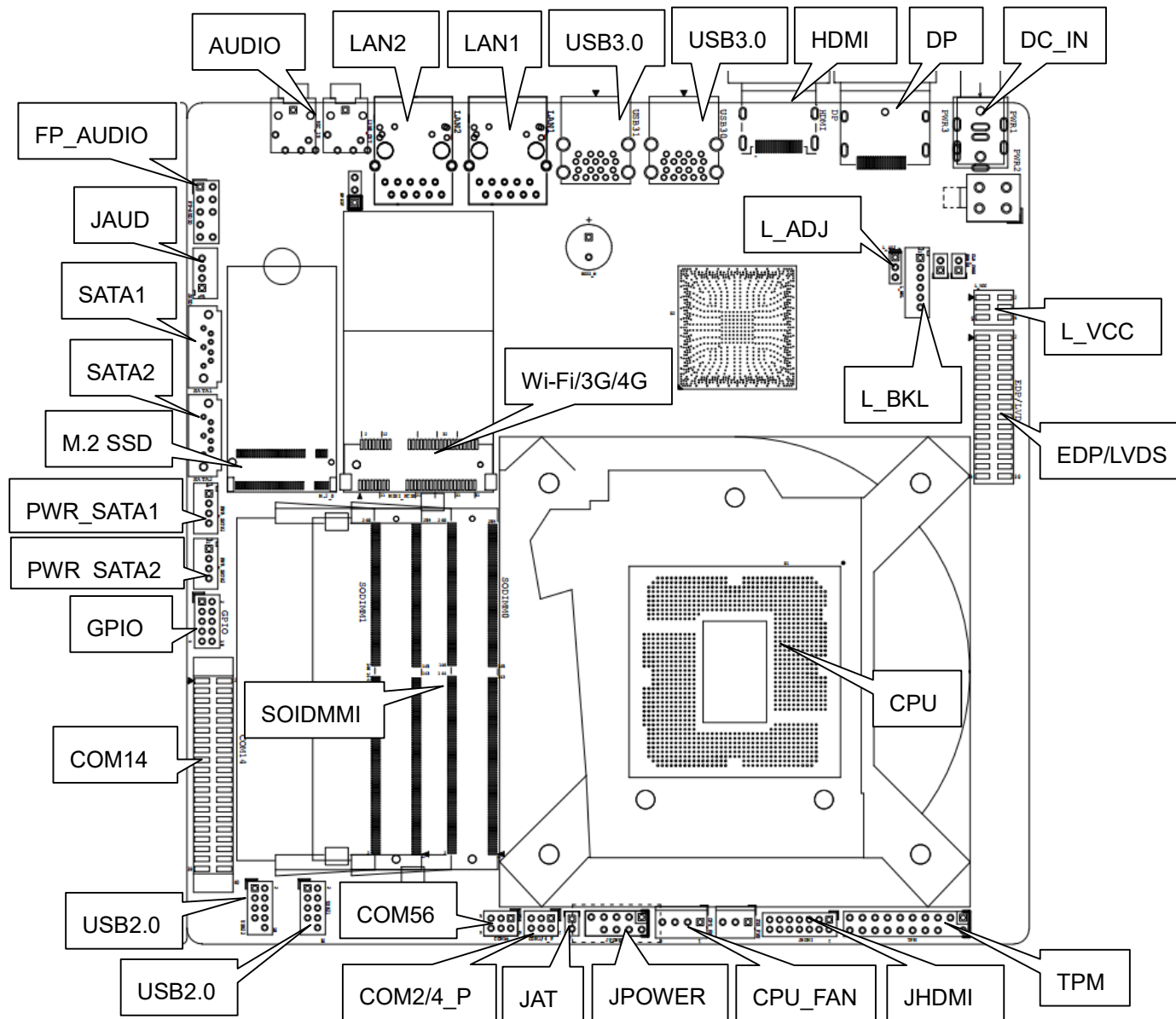
1. Technical Specifications

Processor	CPU	Intel Coffee Lake processors (FCLGA1151)
	Chipset	H310
Memory	Type	2 x SO-DIMM DDR4-2400/2666 MHz
	Max capacity	64 GB
Display	GPU	integrated graphics
	Type	1 x HDMI 1.4, 1x HDMI (pins), 1x DP, 1x LVDS (eDP optional)
Ethernet	Speed	10/100/1000 Mbps
	Controller	RTL8111h
	Interface	2X RJ45
Audio	Audio codec	Realtek HD ALC662
	Interface	Line-out, mic-in, audio header, amplifier header
Hardware		CPU temperature, system temperature, on-board voltage, watchdog
Storage	M.2	1 x M.2_B, supporting 2242 SSD (SATA), 2 x standard SATA3.0
Expansion	PCIe	1x mini PCIe, supporting Wi-Fi and 3G/4G module (optional)
	SIM	1x SIM card slot
I/O	USB	4 x USB3.0
	LAN	2
	HDMI	1
	DP	1
	Audio	1x line-out + 1x mic-in
Internal I/O	COM	4x RS232+2xRS485
	USB	4x USB2.0
	GPIO	8x GPIO
	LVDS	LVDS (eDP optional)
Security	TPM	TPM2.0 on-board, optional
Dimension	Size	170mm x 170mm
Board type		Mini ITX
Power	Standard port	12V DC-in
Temperature	Operating Temp.	-20°C to 60°C
	Storage Temp.	-20°C to 60°C
Cooling method		Passive
Operating System		Windows 10 64bit, Linux 64bit

* All specifications and photos are subject to change without notice.



Connector Diagram



2. Hardware

2.1 Jumper Setting

Please configure the jumpers according to your requirements before installing the hardware.

How to identify the first header of jumpers and pins: Observe the mark beside the jumper or pins and find the header marked by “1” or bold line or triangular symbol. Or observe the rear panel and the header with square solder pad is the first header.

2.2 Memory Slots

On-board 2 x SO-DIMM DDR4-2400/2666 slots, supporting dual channels, maximum capacity 64GB

2.3 Display Interface

1x HDMI 1.4 and optional pin as backup display interface (only one can be connected at one time), 1x DP 1.2, 1x LVDS (eDP1.3 optional). Triple display supporting 4K resolution.

2.3.1 LVDS (mark: EDP/LVDS, L_VCC, L_BKL, L_ADJ)

The board is equipped with dual channel 24bit LVDS interface. The LVDS display power is controlled by the L_VCC jumper, and the LVDS backlight power is controlled by the L_BKL. The backlight two-way control is by L_ADJ.

LVDS data pin (mark: EDP/LVDS)

Signal	Pin		Signal
VCC	1	2	VCC
VCC	3	4	GND
GND	5	6	GND
A_DATA0_DN	7	8	A_DATA0_DP
A_DATA1_DN	9	10	A_DATA1_DP
A_DATA2_DN	11	12	A_DATA2_DP
GND	13	14	GND
A_CLK_DN	15	16	A_CLK_DP
A_DATA3_DN	17	18	A_DATA3_DP
B_DATA0_DN	19	20	B_DATA0_DP
B_DATA1_DN	21	22	B_DATA1_DP
B_DATA2_DN	23	24	B_DATA2_DP
GND	25	26	GND
B_CLK_DN	27	28	B_CLK_DP

Signal	Pin		Signal
B_DATA3_DN	29	30	B_DATA3_DP

Backlight brightness adjustment pin (mark: L_BKL)

Pin	Signal
1	GND
2	GND
3	LCD_BKL_ADJ
4	LCD_BKL_ON
5	12V
6	12V

LVDS display backlight two-way adjustment jumper (mark: L_ADJ)

Pin	Settings	Function
1-2	Close	Backlight control backward
2-3	Close	Backlight control forward

Display power supply jumper (mark: L_VCC)

Interface	Settings	Function
1-2	Close	+3.3V
3-4	Close	+5V
5-6	Close	+12V

Note: The LVDS display power supply is controlled by jumpers. The voltage can be adjusted to 12V, 5V or 3.3V. Don't short-circuit two or more interfaces with jumper cap.

2.3.2 eDP (mark: EDP/LVDS, L_VCC, L_BKL, L_ADJ)

This interface is optional, supporting 2 LANE eDP(1.3). When the interface is set as eDP, LVDS doesn't work. The display power is controlled by the L_VCC jumper, and the LVDS backlight power is controlled by the L_BKL jumper. The backlight two-way control is by L_ADJ.

eDP data pin: (mark: EDP/LVDS)

Signal	Pin		Signal
VCC	1	2	VCC

Signal	Pin		Signal
VCC	3	4	EDP_HPD
GND	5	6	GND
EDP_AUXN	7	8	EDP_AUXP
N/A	9	10	N/A
EDP_DATA0_P	11	12	EDP_DATA0_N
GND	13	14	GND
N/A	15	16	N/A
EDP_DATA1_P	17	18	EDP_DATA1_N
N/A	19	20	N/A
N/A	21	22	N/A
N/A	23	24	N/A
GND	25	26	GND
N/A	27	28	N/A
N/A	29	30	N/A

eDP backlight brightness adjustment pin (mark: L_BKL)

Pin	Signal
1	GND
2	GND
3	LCD_BKL_ADJ
4	LCD_BKL_ON
5	12V
6	12V

eDP backlight two-way control jumper (mark: L_ADJ)

Pin	Settings	Function
1-2	Close	Backlight control backward
2-3	Close	Backlight control forward

eDP display power supply jumper (mark: L_VCC)

Interface	Settings	Function
1-2	Close	+3.3V
3-4	Close	+5V
5-6	Close	+12V

Note: The eDP display power supply is controlled by jumpers. The voltage can be adjusted to 12V, 5V or 3.3V. Don't short-circuit two or more interfaces with jumper cap.

2.4 HDMI pin (mark: JHDMI)

The board is equipped with 1 set of onboard pin HDMI.

JHDMI (mark: JHDMI)

Signal	Pin		Signal
DATA2_P	1	2	DATA2_N
DATA1_P	3	4	DATA1_N
DATA0_P	5	6	DATA0_N
CLK_P	7	8	CLK_N
SCL	9	10	SDA
5V	11	12	GND
HPD	13	14	GND

2.5 Storage interface (mark: SATA1, SATA2, M.2_S)

Supporting 2 standard SATA3.0 interfaces at most, with transmission rate of 6GB/s and two disk power supply socket

M.2 Key B slot (mark: M.2_S) supporting 2242 SSD (SATA).

2.6 USB interface

4 x USB3.0 (rear port), 4x USB2.0 (on-board pins)

USB pins (mark: USB21, USB22)

Signal	Pin		Signal
VCC 5V	1	2	VCC 5V
USB DATA-	3	4	USB DATA-
USB DATA+	5	6	USB DATA+
GND	7	8	GND
(NC)	9	10	N/A

2.7 LAN

The board is equipped with high-performance Gigabyte ethernet controlling chip RTL8111H, with 2 x RJ45 interfaces. Supporting Magic packet wake up. LAN2 supports PXE network boot.

Interface LED indicators:

LILED (green)	Function	ACTLED (orange)	Function
Always on	Network connected	Blinking	Data being transmitted

2.8 Audio interface (mark: FP_AUDIO, JAUD, SPDIF)

ALC662 audio controlling chip is used. The green interface is for audio output (Line_out), and the pink interface is for mic input (Mic-in). The JAUD pin is for power amplifier, and the SPDIF pin is for SPDIF_out.

FP_AUDIO (mark: FP_AUDIO)

Signal	Pin		Signal
MIC2-L	1	2	AGND
MIC2-R	3	4	AVCC
FRO-R	5	6	MIC2-JD
F-IO-SEN(AGNG)	7	8	(NC)
FRO-L	9	10	LIN2-JD

JAUD (mark: JAUD)

Pin	Signal
1	L+
2	L-
3	R-
4	R+

SPDIF (mark: SPDIF)

Pin	Signal
1	+5V
2	SPDIF_Out
3	GND

2.9 Serial port (mark: COM14, COM56, JCOM2/4_P)

It is equipped with 6 COM (2.0mm spacing of built-in pins). COM1 to COM4 are RS232 mode, and COM5-6 is RS485 mode. COM2/4_P provides optional 5V or 12V voltage for COM2 and COM4.

COM14 (mark: COM14)

Signal	Pin		Signal
DCD#	1	2	RXD
TXD	3	4	DTR#
GND	5	6	DSR#
RTS#	7	8	CTS
RI#	9	10	N/A
DCD#	11	12	RXD
TXD	13	14	DTR#
GND	15	16	DSR#
RTS#	17	18	CTS
RI#	19	20	N/A
DCD#	21	22	RXD
TXD	23	24	DTR#
GND	25	26	DSR#
RTS#	27	28	CTS
RI#	29	30	N/A
DCD#	31	32	RXD
TXD	33	34	DTR#
GND	35	36	DSR#
RTS#	37	38	CTS#
RI#	39	40	N/A

COM56 (mark: COM56)

Signal	Pin		Signal
COM5_DATA-	1	2	COM6_DATA-
COM5_DATA+	3	4	COM6_DATA+

Signal	Pin		Signal
GND	5	6	GND

COM2/4 (mark: COM2/4_P)

Interface	Settings	Function
2-4	Close	COM2_5V
4-6	Close	COM2_12V
1-3	Close	COM4_5V
3-5	Close	COM4_12V

2.10 GPIO pin (mark: GPIO)

The board is equipped with a set of 2 x 5pin as JGPIO pin (2.0mm spacing), supporting 8 programmable I/O lanes in total.

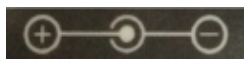
GPIO (mark: JGPIO)

Signal	Pin		Signal
SIO_GP70	1	2	3.3V
SIO_GP71	3	4	SIO_GP74
SIO_GP72	5	6	SIO_GP75
SIO_GP73	7	8	SIO_GP76
GND	9	10	SIO_GP77

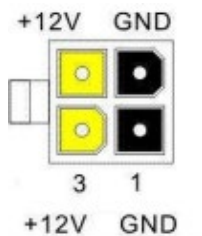
2.11 Board power (mark: PWR1, PWR3)

It supports 12V DC-in power adapter or ATX 12V supplementary power (2 x 2pin).

PWR1: 12V DC-in power socket



PWR3: ATX12V supplementary power supply socket (2x2PIN)



2.12 Switch onboard pin (mark: JPOWER1)

The front control panel interfaces are to connect the functional buttons and indicators on the front panel.

JPOWER1 (mark: JPOWER1)

Signal	Pin		Signal
HDD_LED+	1	2	PWR_LED+
HDD_LED-	3	4	PWR_LED-
RSTBTN-	5	6	PWR_ON+
RSTBTN+	7	8	PWR_ON-
N/A	9	10	(NC)

2.13 TPM (mark: TPM)

TPM (mark: TPM)

Signal	Pin		Signal
CLK	1	2	GND
FRAME#	3	4	(null)
PLTRST#	5	6	+5V
LAD3	7	8	LAD2
+3.3V	9	10	LAD1
LAD0	11	12	GND
SMB_CLK	13	14	SMB_DATA
+3.3V	15	16	SER_IRQ
LPCPD#	17	18	CLK_RUN
GND	19	20	PIRQA#

2.14 Hardware auto start (mark: JAT)

JAT (mark: JAT)

Settings	JAT
Close	Hardware auto start

Please note that this jumper function is similar to the "restore AC power loss" function in BIOS. When

the latter is set to Power on, the device will also start automatically after power is connected.

2.15 CMOS clearance/retention button (mark: CLR_CMOS)

CMOS is powered by the on-board button batteries. Clearing CMOS will permanently remove the previous system settings and restore the board to the original (factory settings) system settings.

Steps:

Step 1: Turn off the PC and disconnect power adapter;

Step 2: Use the jumper cap to connect the 1st and 2nd pins of CLR_CMOS for about 10 seconds and disconnect;

Step 3: When starting the device, press the button to enter the BIOS, load the optimal default value and save and exit the settings.

COMS (mark: CLR_CMOS)

Settings	CLR_CMOS
Close	Clear the CMOS

 Don't clear COMS when the PC is connected to power in case the board is damaged.